(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 0 822 578 A1

(12) EUROPEAN PATENT APPLICATION

(43) Date of publication:
04.02.1998 Bulletin 1998/06

(21) Application number: 96830436.0

(22) Date of filing: 31.07.1996

(51) Int. Cl.[6]: H01L 21/00, H01L 21/762, H01L 21/764, G01L 9/00, G01N 27/12

(84) Designated Contracting States:
DE FR GB IT

(71) Applicant:
SGS-THOMSON MICROELECTRONICS s.r.l.
20041 Agrate Brianza (Milano) (IT)

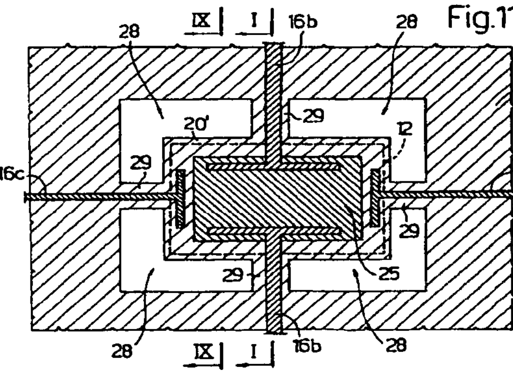
(72) Inventors:
- Villa, Flavio
20159 Milano (IT)
- Ferrari, Paolo
21013 Gallarate (IT)
- Vigna, Benedetto
85100 Potenza (IT)

(74) Representative:
Cerbaro, Elena et al
STUDIO TORTA S.r.l.,
Via Viotti, 9
10121 Torino (IT)

(54) Method of fabricating integrated semiconductor devices comprising a chemoresistive gas microsensor

(57) The chemoresistive gas sensor comprises a heating element (12) integrated in a dedicated SOI substrate (100) having an air gap (3) in the intermediate oxide layer (2) between two wafers (1, 4) of monocrystalline silicon; the sensitive element (25) of tin oxide is formed over the heating element and separated from it by a dielectric insulating and protective layer. A trench (28), formed at the end of the fabrication of the device, extends from the surface (6) of the wafer (4) in which the heating element (12) is integrated, up to the air gap (3) to mechanically separate and insulate the sensitive element (25) from the rest of the chip, and so improve the mechanical characteristics, sensitivity and response of the sensor.

Fig.11



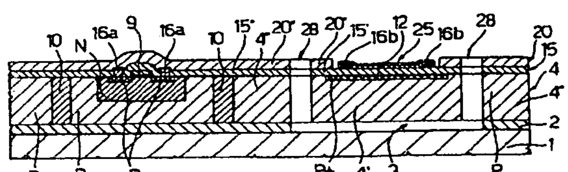


Fig.10

EP 0 822 578 A1

Printed by Xerox (UK) Business Services
2.15.8/3.4

Description

The present invention relates to a method of fabricating integrated semiconductor devices comprising a chemoresistive gas microsensor.

As is known, chemical sensors detect the presence of gas by virtue of a chemical reaction between the molecules of the gas and a sensitive film. The chemical reaction depends to a large extent on operating temperature, which affects adsorption, desorption and diffusion of the gas in the film, and is therefore an important factor in optimizing performance of the sensor, particularly in terms of sensitivity, selectivity and response time. Thus, for optimizing the operation sensors are equipped with temperature regulating and control means.

In recent times, integrated chemoresistive gas microsensors have been fabricated using microelectronics technology. Such sensors present numerous advantages: low fabrication cost; low in-service energy consumption; rapid response time; and integration with the temperature control and output signal processing circuit.

Integrated gas microsensors which are now being marketed feature chemoresistive tin oxide diaphragms deposited on a wafer of bulk-micromachined semiconductor material, and detect the presence of gas as a change in the resistance of the film caused by a chemical reaction, on the surface of the diaphragm, between the oxygen of the diaphragm and the gas.

As such sensors, to function properly, must be maintained at a temperature of about 400°C, they are provided with heating elements and must be isolated thermally from the rest of the chip integrating the signal control and processing circuit.

Various techniques are known for isolating the sensitive portion from the rest of the chip, the traditional one being bulk micromachining, which consists in forming the sensitive portion on or in a dielectric layer deposited on a massive silicon wafer, and in removing a portion of the massive silicon from the rear of the wafer by plasma or wet etching. The dielectric layer performs the dual function of mechanically supporting the sensor, and thermally isolating it from the massive silicon wafer. Using this technique, prototypes have been formed wherein part of the silicon is removed from the sensor area and only part of the thickness of the wafer is etched, wherein, in other prototypes, all the silicon is removed at the sensor area (etching extending up to the dielectric layer supporting the sensor element). Details of the latter solution are to be found, for example, in the article entitled "Basic micro-module for chemical sensors with on-chip heater and buried sensor structure" by D. Mutschall, C. Scheibe and E. Obermeier.

Bulk micromachining, however, requires front-rear processing and such particular handling of the wafers as to be incompatible with current integrated circuit fabrication methods.

Another technique is front micromachining, whereby the massive silicon wafer or a sacrificial layer is etched from the front, and a dielectric layer mechanically supports and thermally isolates the sensor element. Details of this technique, relative to the fabrication of a different type of sensor, are to be found in the article entitled "A high-sensitivity CMOS gas flow sensor based on an N-poly/P-poly thermopile" by D. Moser and H. Baltes, DSC-Vol 40, Micromechanical Systems, ASME, 1992. And a general review of bulk and front micromachining technology is to be found in the article entitled "Micromachining and ASIC technology" by Axel M. Stoffel, Microelectronics Journal, 25 (1994), p. 145-156.

Forming suspended structures using this technique, however, involves etching steps which are incompatible with current microelectronics fabrication processes, so that the sensors and relative control and processing circuits cannot be formed on one chip.

For sensors of a different type, dedicated SOI (Silicon-on-Insulator) substrates have been proposed, wherein the starting wafer comprises a Silicon-Silicon Oxide-Silicon stack with the oxide selectively removed at the sensor area to form an air gap. The trenches formed from the front of the wafer after contacting the air gap provide for thermally isolating the sensor. Details of this technique, relative to a shear stress sensor, are to be found, for example, in the article entitled "A Microfabricated Floating-Element Shear Stress Sensor Using Wafer-Bonding Technology" by J. Shajii, Kay-Yip Ng and M.A. Schmidt, Journal of Microelectromechanical Systems, Vol. 1, N. 2, June 1992, p- 89-94. The bonding technique used (excluding formation of the air gap) is also described in the article entitled "Silicon-on-Insulator Wafer Bonding-Wafer Thinning Technological Evaluations" by J. Hausman, G.A. Spierings, U.K.P. Bierman and J.A. Pals, Japanese Journal of Applied Physics, Vol. 28, N. 8, August 1989, p. 1426-1443.

It is an object of the present invention to provide a fabrication method and chemoresistive gas sensor designed to overcome the drawbacks typically associated with known technology.

According to the present invention, there are provided a method of fabricating an integrated semiconductor device comprising a chemoresistive gas microsensor, and an integrated device comprising a chemoresistive gas microsensor, as claimed respectively in Claims 1 and 12.

In practice, according to the present invention, the sensor is formed using a SOI substrate; and the heating element and sensitive element are respectively integrated in and formed on the substrate, and are isolated from each other by a dielectric to provide for improved mechanical characteristics, greater sensitivity and more rapid response as compared with known sensors.

A preferred, non-limiting embodiment of the present invention will be described by way of example with reference to the accompanying drawings, in which:

Figures 1 to 8 show cross sections of a semiconductor material wafer at successive steps in the fabrication method according to the present invention;

Figures 9 and 10 show cross sections in a different plane from that of Figures 1-8, at successive steps in the fabrication method according to the invention;

Figure 11 shows a larger-scale top plan view of a portion of the Figure 10 wafer.

In the present fabrication method, a silicon oxide layer 2 is formed, e.g. grown thermally, on a first wafer 1 of monocrystalline silicon (Figure 1); oxide layer 2 is masked and etched to selectively remove a portion thereof and form an opening 3 to later form an "air gap" (Figure 2); and a second wafer 4 of monocrystalline silicon, P-type in the example shown, is bonded to oxide layer 2 using, for example, the method described in the above article by J. Hausman, G.A. Spierings, U.K.P. Bierman and J.A. Pals, to form a dedicated SOI substrate 100 in which the air gap 3 is defined at the top and bottom by second and first wafers 4 and 1, and laterally by oxide layer 2.

At this point, SOI substrate 100 is processed as usual for forming integrated circuit bipolar and MOS electronic components. More specifically (Figure 4), in second wafer 4, there are formed junction or dielectric insulating regions 5 extending from upper surface 6 of second wafer 4 to oxide layer 2, and a PMOS transistor formed in an N-well 7 and presenting P-type source and drain regions 8, and a control gate region 9 insulated from second wafer 4 by a gate oxide region 14. Figure 4 also shows (schematically by arrows 11) self-aligned implanting of source and drain regions 8 using a resist mask 10, in the course of which, a region 12 forming the heater of the gas sensor is also implanted, preferably, as shown in Figure 4, through a protective oxide layer 13 covering surface 6 of second wafer 4.

A dielectric protective layer 15 (e.g. of silicon nitride or BPSG - Boron Phosphorous Silicon Glass) is then deposited, which also provides for electrically insulating the heater from the sensitive element; the contacts are opened; and a metal layer 16 is deposited to form the contact electrodes (Figure 5). Metal layer 16 may comprise a triple titanium-platinum-chromium layer or a single tungsten layer to permit higher operating temperatures of the finished device than those withstandable by an aluminium layer.

Metal layer 16 is then defined to form, on second wafer 4, metal contact regions 16a for electronic component regions 8, 9, 16b for the sensitive element, and 16c (shown only in Figure 11) for region 12 forming the heater. A dielectric (e.g. TEOS - tetraethylorthosilicate) masking layer 20 is deposited and removed at the region in which the sensitive element is to be formed, to obtain the intermediate structure shown in Figure 6.

At this point, a tin oxide film 21 is deposited (e.g. by sputtering) and, over this, a platinum-palladium catalyst layer 22 to reduce the energy required to activate sensitive film 21 and assist the chemical reaction between the gas molecules and tin oxide (Figure 7).

A resist mask 24 is then deposited for defining tin oxide film 21 and catalyst layer 22, and so obtain the intermediate structure shown in Figure 8, in which the remaining portions of film 21 and layer 22 form the sensitive element 25. At this point, mask 24 is removed, and a trench is excavated, surrounding all sides (except for connection portions) of the region of second wafer 4 supporting sensitive element 25. To this end, a resist mask 26 is deposited (see Figure 8, which, in the sensor region, shows a different section from that in Figures 1-7); using mask 26 portions of dielectric masking layer 20, of dielectric protective layer 15, and of second wafer 4 up to air gap 3 are removed, thereby forming trench 28, as shown in Figure 9. Trench 28 preferably extends along a closed line, e.g. the sides of a rectangle (as shown in Figure 11 in which dielectric protective layer 20 is removed) or along the circumference of a circle, so as to laterally define an inner portion 4' of second wafer 4; and advantageously extends along the periphery of air gap 3. Trench 28 comprises a number of portions separated by connecting and supporting arms 29 extending between inner portions 4', 15', 20' and respective outer portions 4", 15", 20" of wafer 4 and dielectric layers 15, 20 (Figure 9) so that inner portion 4' is thermally isolated from the rest of the chip. Mask 26 is then removed to obtain the final structure shown in section in Figure 10 and from above in Figure 11.

The advantages of the fabrication method and sensor according to the present invention are as follows.

Using a SOI substrate 100, the method described is fully compatible with planar microelectronics technology, thus enabling the same advantages in terms of reliability, reproducibility and cost, as well as enabling the sensor and relative signal control and processing circuits to be integrated on one chip.

Moreover, as compared with known solutions involving anisotropic etching from the front or rear of the substrate, spatial integration of the sensor is improved, so that the sensor is smaller and requires less energy for it to operates as compared with known sensors.

Forming the heater of monocrystalline silicon, instead of polysilicon, provides for a more uniform and faster heating of the sensor element 25. Indeed, the more uniform heating causes an improved selectivity and sensitivity of the sensor, while the faster heating reduces the response time of the sensor, giving rise to an improved operation thereof. And finally, the mechanical stability of the sensor is improved (Young and Poisson moduli less dependent on process parameters as compared with deposited films).

Clearly, changes may be made to the fabrication method and sensor as described and illustrated herein without, however, departing from the scope of the present invention. More specifically, the isolating regions in the second wafer may be of a different type, e.g. dielectric type instead of junction type; the elec-

tronic components integrated in the same chip may be both bipolar and MOS; the conductivity types of the various regions may be other than as shown; and the catalyst layer may be omitted.

Claims

1. A method of fabricating integrated semiconductor devices comprising chemoresistive gas microsensors, characterized by the steps of:

   - forming a SOI substrate (100) of semiconductor material;
   - forming a heating element (12) in said SOI substrate; and
   - forming a gas-sensitive element (25) on said SOI substrate (100).

2. A method as claimed in Claim 1, characterized in that said step of forming a SOI substrate comprises the steps of:

   - forming an insulating material layer (2) on a first wafer (1) of monocrystalline semiconductor material;
   - selectively removing a portion of said insulating material layer (2); and
   - bonding a second wafer (4) of monocrystalline semiconductor material to said insulating material layer, so as to define an air gap (3) together with said first wafer and said insulating material layer.

3. A method as claimed in Claim 2, characterized in that said step of forming a gas-sensitive element (25) is followed by the step of selectively removing portions of said second wafer (4) to form a trench (28) extending from a surface (6) of said second wafer to said air gap (3).

4. A method as claimed in Claim 3, characterized in that said trench (28) comprises a number of trench portions extending substantially in a closed line along the periphery of said air gap (3); said trench portions being mutually separated by connecting and supporting arms (29) formed by said second wafer (4).

5. A method as claimed in any one of Claims from 2 to 4, characterized in that said step of forming a heating element (12) comprises the step of implanting said SOI substrate (100) with a doping agent in a portion over said air gap (3).

6. A method as claimed in Claim 5, characterized in that said step of implanting said SOI substrate (100) is performed simultaneously with a step of implanting a conductivity region (8) of an integrated electronic component.

7. A method as claimed in any one of Claims from 2 to 4, characterized in that said step of forming a heating element (12) comprises the step of implanting said second wafer (4) in a portion over said air gap (3); and in that said step of forming a gas-sensitive element (25) comprises the steps of forming a protective region (15') of insulating material over said second wafer (4), and forming a sensitive region (25) of gas-sensitive material over said protective region.

8. A method as claimed in any one of Claims from 1 to 6, characterized in that said step of forming a gas-sensitive element (25) comprises the steps of:

   - forming a protective layer (15) of insulating material on said SOI substrate (100); and
   - forming a sensitive region (25) of gas-sensitive material over said protective layer (15).

9. A method as claimed in Claim 8, characterized in that said step of forming a protective layer (15) on said SOI substrate (100) is followed by the steps of:

   - opening contact portions in said protective layer (15);
   - depositing a metal material layer (16) over said protective layer (15); and
   - defining said metal material layer (16);

   and in that said step of forming a sensitive region (25) comprises the steps of:

     - forming a masking structure (20) presenting a window over said heating element (12);
     - depositing a layer (21, 22) of said gas-sensitive material; and
     - defining said layer of gas-sensitive material.

10. A method as claimed in Claim 9, characterized in that said step of depositing a metal material layer (16) comprises the step of depositing a triple layer of titanium, platinum and chromium.

11. A method as claimed in Claim 9, characterized in that said step of depositing a metal material layer (16) comprises the step of depositing a layer of tungsten.

12. An integrated semiconductor device comprising a semiconductor material substrate (100), and a chemoresistive gas microsensor including a heating element (12) and a gas-sensitive element (25); characterized in that said semiconductor material substrate is a SOI substrate (100), and said heating

element (12) is integrated in said SOI substrate.

13. A device as claimed in Claim 12, characterized in that said SOI substrate (100) comprises a first wafer (1) of monocrystalline semiconductor material; an insulating material layer (2) over said first wafer (1); and a second wafer (4) of monocrystalline semiconductor material over said insulating material layer (2); said insulating material layer being interrupted at an air gap (3) defined by said first and second wafers (1, 4) and by said insulating material layer (2).

14. A device as claimed in Claim 13, characterized by comprising a trench (28) extending from a surface (6) of said second wafer (4) to said air gap (3).

15. A device as claimed in Claim 12, characterized in that said trench (28) comprises a number of trench portions extending substantially in a closed line along the periphery of said air gap (3); said trench portions being mutually separated by connecting and supporting arms (29) formed by said second wafer (4).

16. A device as claimed in any one of Claims from 13 to 15, characterized in that said heating element (12) comprises a region implanted with a doping agent in a portion of said second wafer (4) over said air gap (3).

17. A device as claimed in Claim 16, characterized by a protective region (15) of insulating material extending over a surface (6) of said second wafer (4) over said implanted region (12); and a sensitive region (25) of gas-sensitive material extending over part of said protective region (15).

18. A device as claimed in Claim 17, characterized by contact regions (16c, 16b, 16a) of metal material connected electrically to said implanted and sensitive regions (12, 25) and to conductivity regions (8) of an integrated electronic component; and in that said metal material comprises a triple layer of titanium, platinum and chromium.

19. A device as claimed in Claim 17, characterized by contact regions (16c, 16b, 16a) of metal material connected electrically to said implanted and sensitive regions (12, 25) and to conductivity regions (8) of an integrated electronic component; and in that said metal material comprises a layer of tungsten.

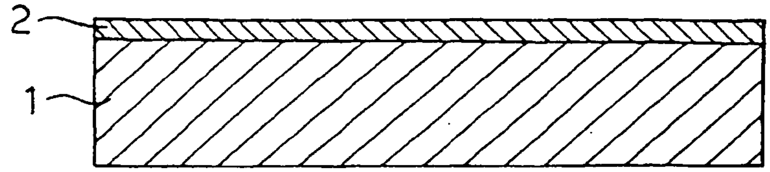


Fig.1

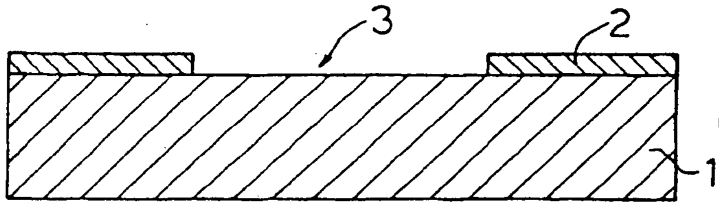


Fig.2

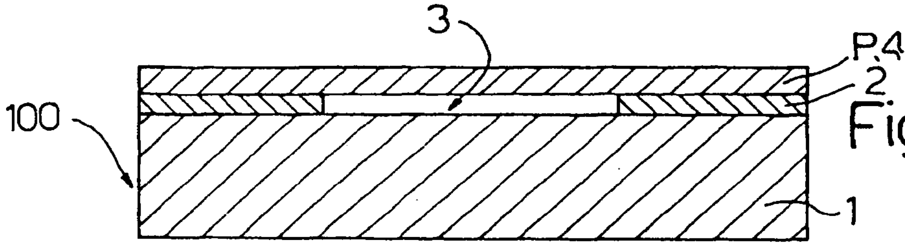
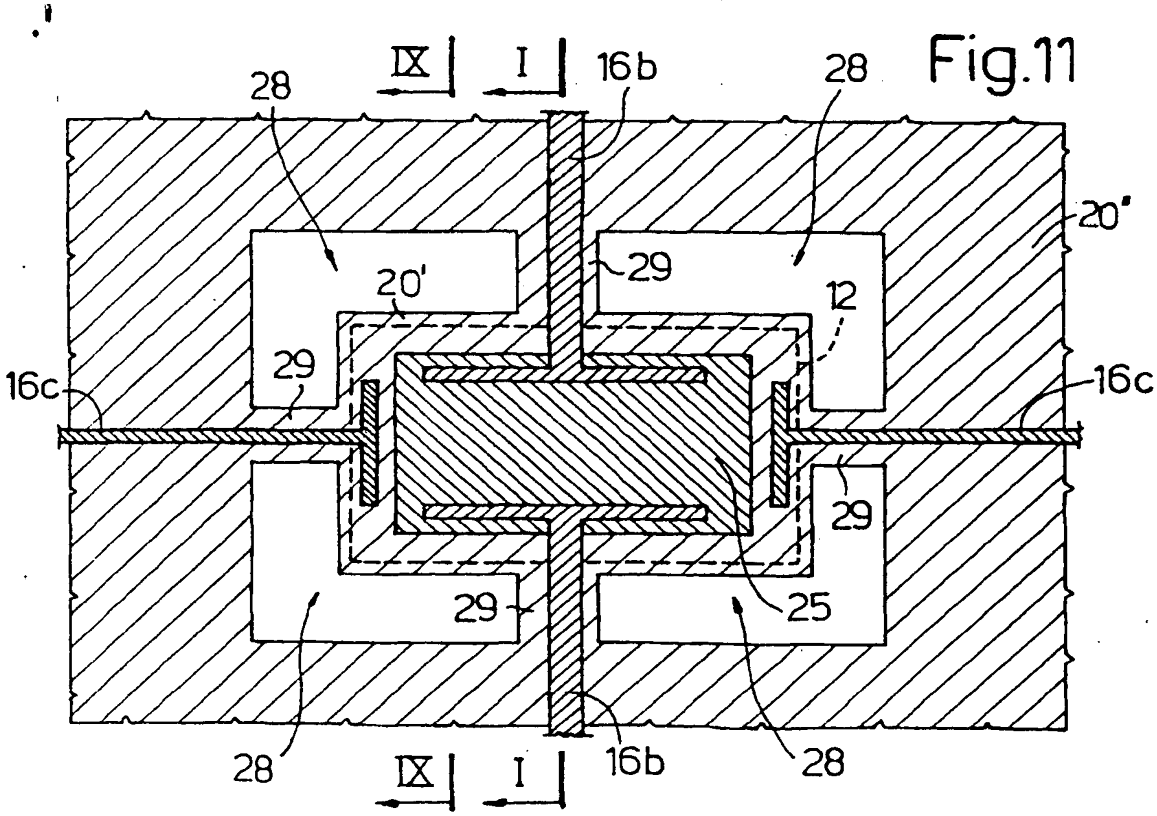


Fig.3

Fig.11



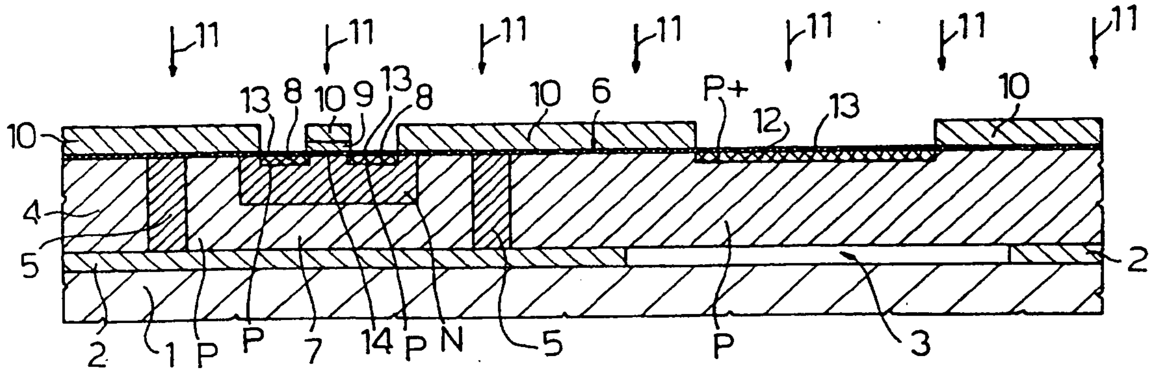


Fig.4

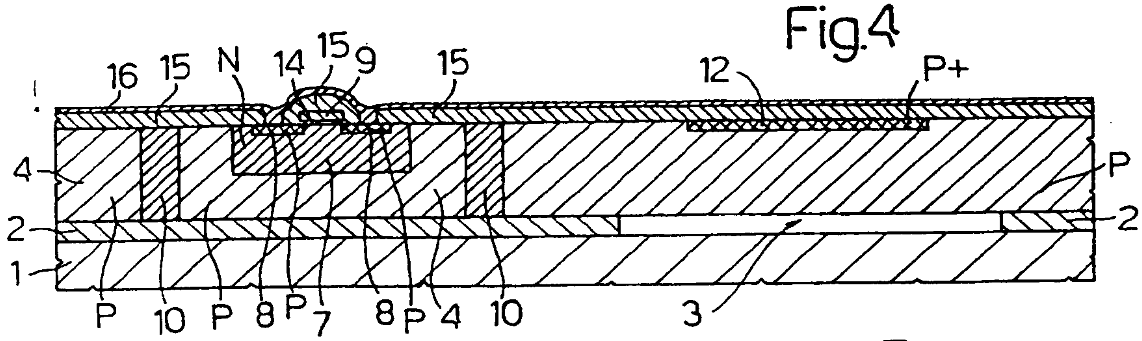


Fig.5

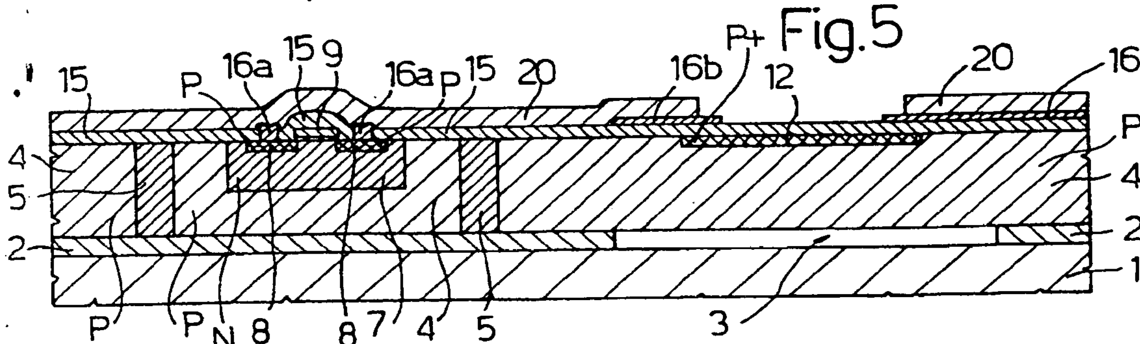


Fig.6

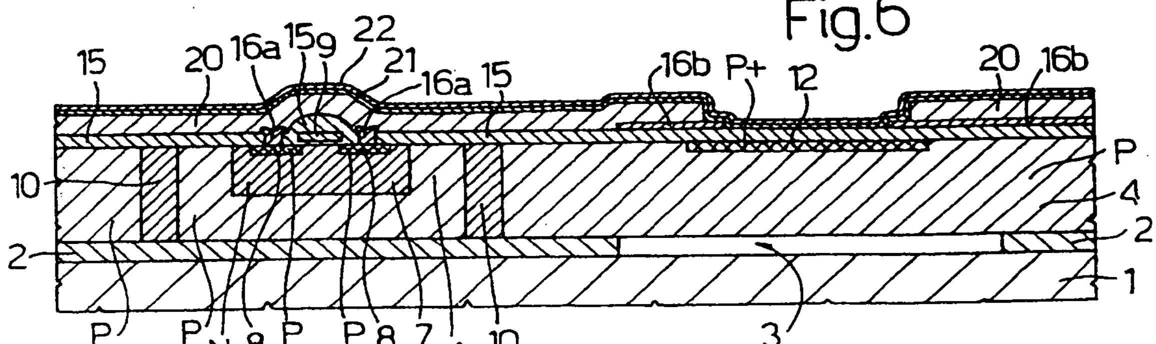


Fig.7

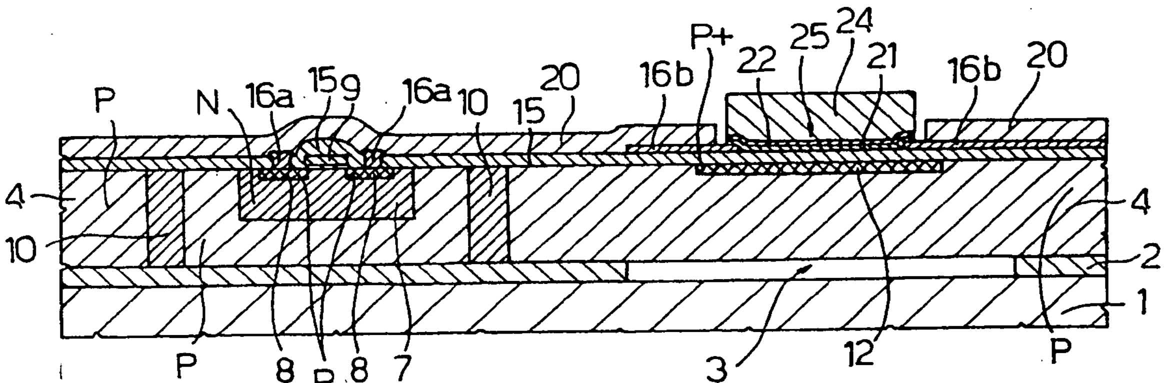


Fig.8

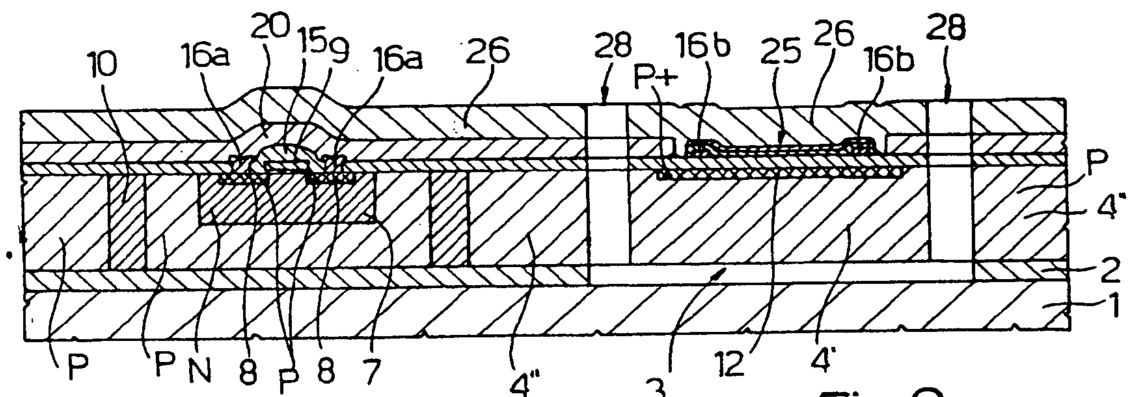


Fig.9

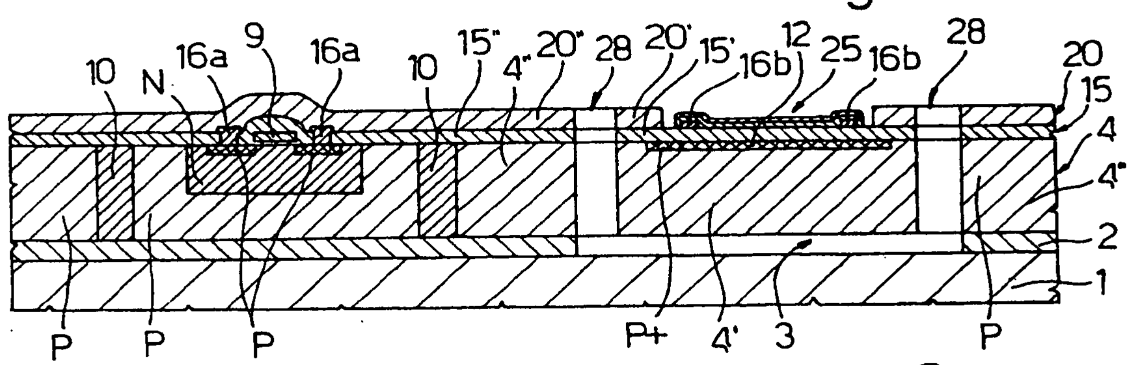


Fig.10

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 96 83 0436

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
A	US-A-4 580 439 (MANAKA JUNJI) 8 April 1986 * the whole document * ---	1-4,8-15	H01L21/00 H01L21/762 H01L21/764 G01L9/00 G01N27/12
D,A	JOURNAL OF MICROELECTROMECHANICAL SYSTEMS, JUNE 1992, USA, vol. 1, no. 2, ISSN 1057-7157, pages 89-94, XP000615062 SHAJII J ET AL: "A microfabricated floating-element shear stress sensor using wafer-bonding technology" ---	1,2, 12-14	
A	EP-A-0 346 127 (VAISALA OY ;KEMIRA OY (FI); NESTE OY (FI); OUTOKUMPU OY (FI); ENGI) 13 December 1989 * the whole document * ---	1-4,12	
A	WO-A-95 10770 (CSIR ;VYVER JAMES EDWARD VAN DE (ZA); BRODALKA MARYSIA (ZA); HOWDE) 20 April 1995 * the whole document * ---	1-4,8-15	
D,A	8TH INTERNATIONAL CONFERENCE ON SOLID-STATE SENSORS AND ACTUATORS AND EUROSENSORS IX. DIGEST OF TECHNICAL PAPERS (IEEE CAT. NO.95TH8173), PROCEEDINGS OF THE INTERNATIONAL SOLID-STATE SENSORS AND ACTUATORS CONFERENCE - TRANSDUCERS `95, STOCKHOLM, SWED, ISBN 91-630-3473-5, 1995, STOCKHOLM, SWEDEN, FOUND. SENSORS & ACTUATOR TECHOL, SWEDEN, pages 256-259 vol.1, XP000612710 MUTSCHALL D ET AL: "Basic micro module for chemical sensors with on chip heater and buried sensor structure" ---	1,12	TECHNICAL FIELDS SEARCHED (Int.Cl.6) H01L G01L G01P G01N G01B
A	US-A-5 242 863 (XIANG-ZHENG TU ET AL) 7 September 1993 * the whole document * --- -/--	1-4, 12-15	

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	20 December 1996	Brock, T

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 96 83 0436

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
A	US-A-5 510 276 (DIEM BERNARD ET AL) 23 April 1996 * the whole document * -----	1-4, 12-15	

TECHNICAL FIELDS SEARCHED (Int.Cl.6)

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	20 December 1996	Brock, T

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P04C01)